WHAT IS CLAIMED IS:

Sub A1

1. A memory arrangement comprising:

a programmable memory;

a first buffer memory associated with the programmable memory, to which first buffer memory, in the case of a command access, at least one command following the accessed command is written; and

a second buffer memory to which, in the case of a data access, at least one datum following the accessed datum is written.

2. The memory arrangement according to claim 1, wherein the programmable memory includes a burst flash memory.

3. The memory arrangement according to claim 1, wherein the second buffer memory is loaded only in the case of a data access.

4. The memory arrangement according to claim 1, wherein content of the first buffer memory is not changed when the at least one datum is subsequently read from the second buffer memory.

5. A method for performing at least one of a command access and a data access during a program execution in connection with a programmable memory, comprising the steps of:

recognizing in the case of a command access that a command access is present;

recognizing in the case of a data access that a data access is present;

writing a command following the accessed command to a first buffer memory; and

writing a datum following the accessed datum to a second buffer memory.

6. The method according to claim 5, further comprising the step of:

shifting access to the programmable memory between the first buffer memory and the second buffer memory as a function of whether the command access or the data access is desired.

7. The method according to claim 6, wherein the step of shifting access is determined by an address matcher that recognizes whether the command access or the data access is desired.

8. The method according to claim 6, wherein the step of shifting access is determined by at least one signal of a processor which indicates whether the command access or the data access is desired.